REMARKS

Repacement drawings are submitted herewith to satisfy the draftperson's objections.

Claims 6 and 19 have been canceled.

New Claim 20 has been added.

The claims have been amended as suggested by the examiner to overcome the objections and not to satisfy a statutory requirement. Support for the amendment may be found in the original claims and from the description of fig. 4 on page 10, lines 4-10; page 15, lines 5-27; and from page 18, line 2 to page 20, line 5 of the specification.

Claims 1-5, 7-18 and 20 remain pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Leo J. Peters at (408)433-4578 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 USC § 102(e)

Claims 1-5 and 7-18 stand rejected under 35 USC § 102(e) as being anticipated by Petranovic et al., U.S. Patent 6,546,541 B1 (*Petranovic*). Applicant traverses the rejection as follows.

As attested to in the attached Declaration under 37 C.F.R. § 1.131, Applicants are the co-inventors of the invention disclosed and claimed in the subject application, and Applicants disclosed the invention disclosed in the attached invention disclosure to LSI Logic Corporation for

"OPTIMIZED REPEATER INSERTION" before the filing date of February 20, 2001, of U.S. Patent Application US 6,546,541 B1 by Petranovic, et al. The copy of the disclosure attached does not include the date and signature of the inventors because the file containing the original executed disclosure was lost, as declared to by Mark Salvatore in the attached declaration under 37 C.F.R. § 1.132. The declaration under 37 C.F.R. § 1.132 further attests to the evidence that the invention disclosure was received by LSI Logic Corporation before the effective date of the reference as documented in the attached copy of the electronic database entry.

Because Applicants invented the subject matter of the rejected claims prior to the effective date of the reference, the rejection under 35 USC § 102(e) is overcome. Further, the rejection errs as explained below.

As described in column 7, lines 61-65 cited by the rejection, *Petranovic* discloses generating a capacitance constraint for each net driver using a re-synthesis algorithm to ensure that timing constraints are satisfied, that is, the capacitance constraints are generated for each driving cell rather than being retrieved from a lookup table. In contrast to the re-synthesis algorithm disclosed in *Petranovic*, Claims 1 and 10 recite retrieving a previously defined critical net length associated with the driving cell and the interconnect from a library lookup table. Because *Petranovic* lacks the claimed step of retrieving a previously defined critical net length associated with the driving cell and the interconnect from the claimed library lookup table and the claimed step of comparing a net length of the interconnect with the previously defined critical net length, *Petranovic* does not anticipate Claims 1 and 10 under 35 USC § 102(e).

In column 5, lines 1-14 and 22-44 cited by the

rejection, *Petranovic* discloses a physical delay calculator to identify critical paths and insertion of buffers using a re-synthesis algorithm, that is, the critical path lengths are calculated by the re-synthesis algorithm. In contrast to *Petranovic*, Claims 1 and 10 recite comparing a net length of the interconnect with a previously defined critical net length from the claimed library lookup table. If the interconnect length exceeds the previously defined critical net length, then a buffer cell is selected from the library lookup table to meet a given performance constraint for the interconnect. Because *Petranovic* lacks the claimed step of comparing a net length of the interconnect with a previously defined critical net length, *Petranovic* does not anticipate Claims 1 and 10 under 35 USC § 102(e).

In column 8, lines 33-43 cited by the rejection, *Petranovic* discloses inserting buffers or buffer trees in critical paths using the re-synthesis algorithm to ensure that a performance constraint is met. In contrast to using a re-synthesis algorithm as disclosed in *Petranovic*, Claims 1 and 10 recite selecting a buffer cell from the library lookup table to ensure that a performance constraint is met. Because *Petranovic* lacks the claimed selecting a buffer cell from the library lookup table to ensure that a performance constraint is met, *Petranovic* does not anticipate Claims 1 and 10 under 35 USC § 102(e).

In column 7, lines 29-31 cited by the rejection, *Petranovic* discloses a library table for determining an output ramp time as a function of total capacitance. However, *Petranovic* ensures that the performance constraint defined by the maximum allowable ramp time specification is met by applying the re-synthesis algorithm to the output ramp time in lines 34-60. In contrast to *Petranovic*, Claims 1 and 10

recite selecting a buffer cell from the library lookup table to meet a given performance constraint for the interconnect. Because *Petranovic* lacks the claimed selecting a buffer cell from the library lookup table to meet a given performance constraint for the interconnect, *Petranovic* does not anticipate Claims 1 and 10 under 35 USC § 102(e).

In column 6, line 52 to column 7 line 65 and column 8, lines 43-67 cited by the rejection, *Petranovic* discloses determining interconnect capacitance and ensuring that a performance constraint is met using a re-synthesis algorithm. In contrast to the re-synthesis algorithm disclosed in *Petranovic*, Claims 1 and 10 recite retrieving a previously defined critical net length associated with the driving cell and the interconnect from a library lookup table. Because *Petranovic* lacks the claimed step of retrieving a previously defined critical net length associated with the driving cell and the interconnect from the claimed library lookup table and the claimed step of comparing a net length of the interconnect with the previously defined critical net length, *Petranovic* does not anticipate Claims 1 and 10 under 35 USC § 102(e).

In column 6, line 22 to column 7, line 65 and column 8, lines 43-67 cited by the rejection, *Petranovic* discloses estimating an interconnect delay for each net. In contrast to the estimation algorithm disclosed in *Petranovic*, Claims 1 and 10 recite retrieving a previously defined critical net length associated with the driving cell and the interconnect from a library lookup table. Because *Petranovic* lacks the claimed step of retrieving a previously defined critical net length associated with the driving cell and the interconnect from the claimed library lookup table, *Petranovic* does not anticipate Claims 1 and 10 under 35 USC § 102(e).

Applicant respectfully requests examination and favorable reconsideration of Claims 1-5 and 7-18.

No additional fee is believed due for this amendment.

Respectfully submitted,

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encl:

(1) Declaration under 37 C.F.R. § 1.131

(2) Declaration of Mark Salvatore under 37 C.F.R. § 1.132

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